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Bandwidth Limited Sampling Circuit of High Linearity

Abstract

A bandwidth limited sampling circuit of high linearity may be implemented by using a first circuit portion to limit the bandwidth of the input signals, and using a second circuit portion to sample the bandwidth limited input signal. The first circuit portion and the second circuit portion may be implemented using separate components. In an alternative embodiment, bandwidth limiting is implemented by taking a difference of a sampled input signal from a sampled high frequency components of the input signal.